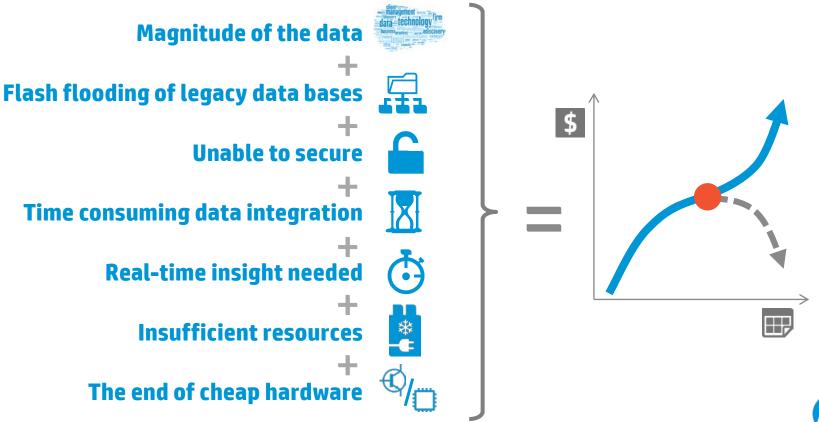


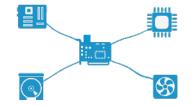
The Machine: The future of technology

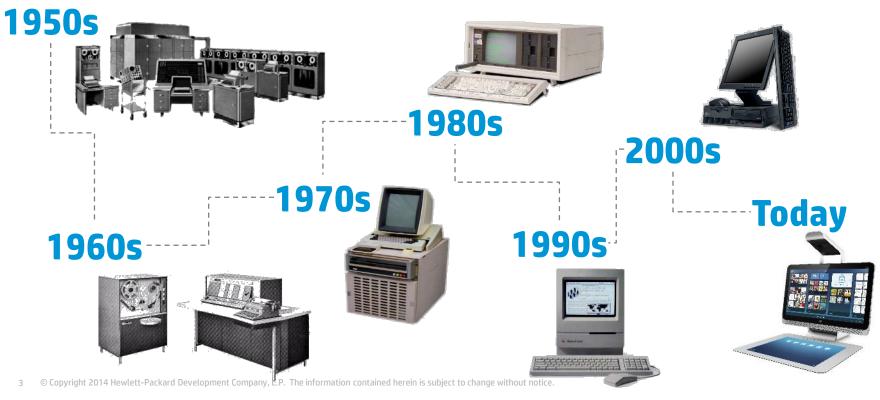
HP Labs

What are the questions you can't ask today?

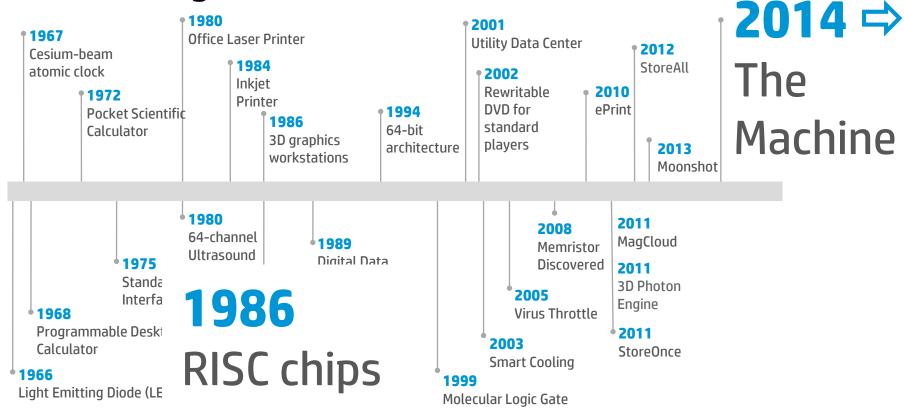


The Past 60 Years

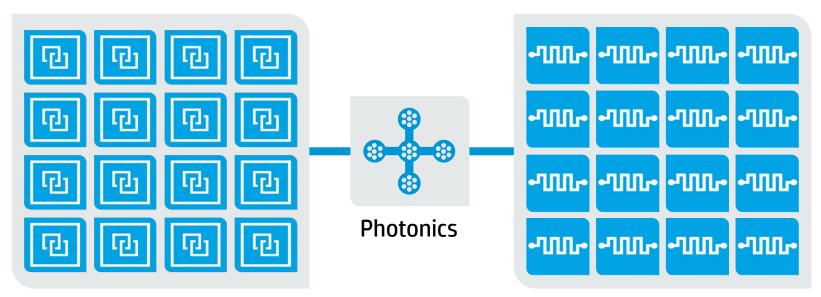




HP Labs: engine of innovation





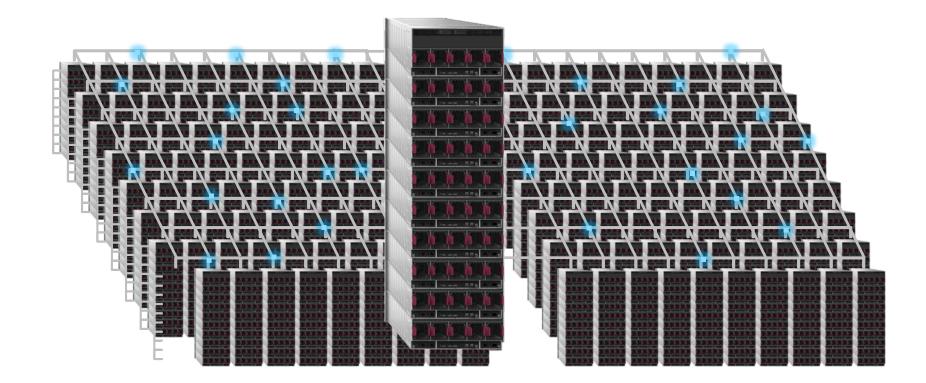


Special purpose cores

Massive memory pool

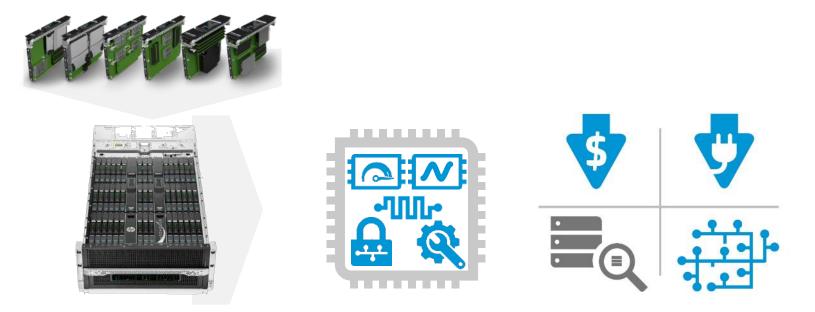
The Machine





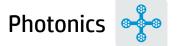






Customize the hardware to the workload

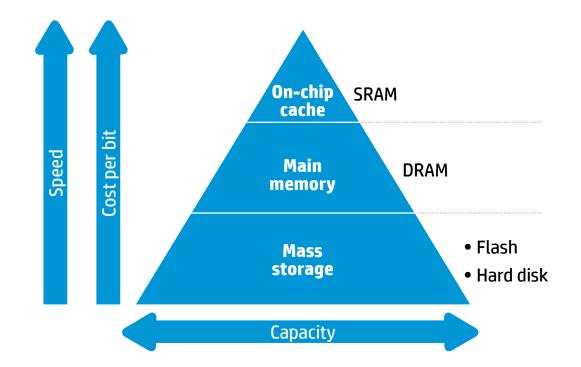






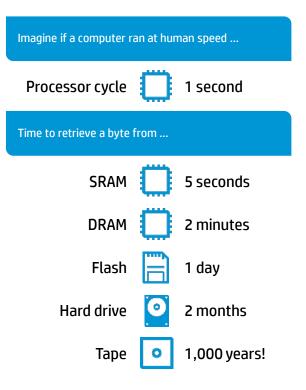
Photonics destroys distance

Massive memory pool

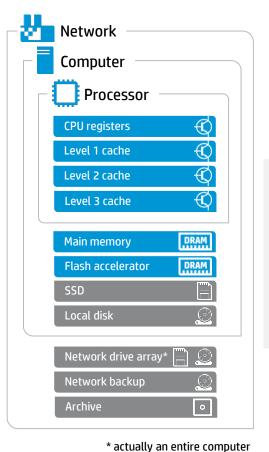


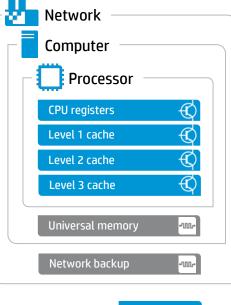
Universal memory obsoletes this hierarchy







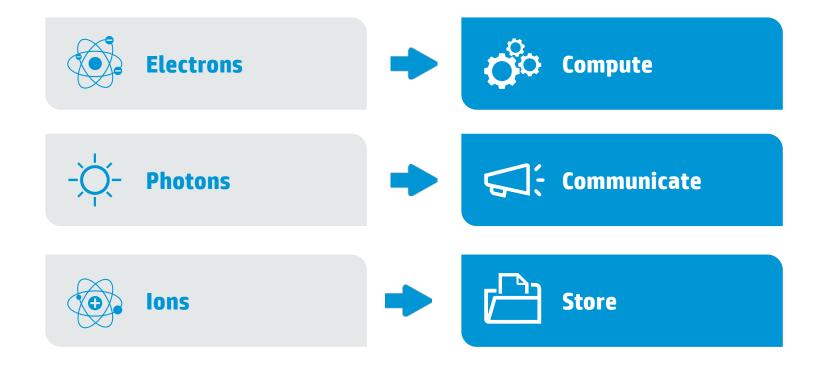




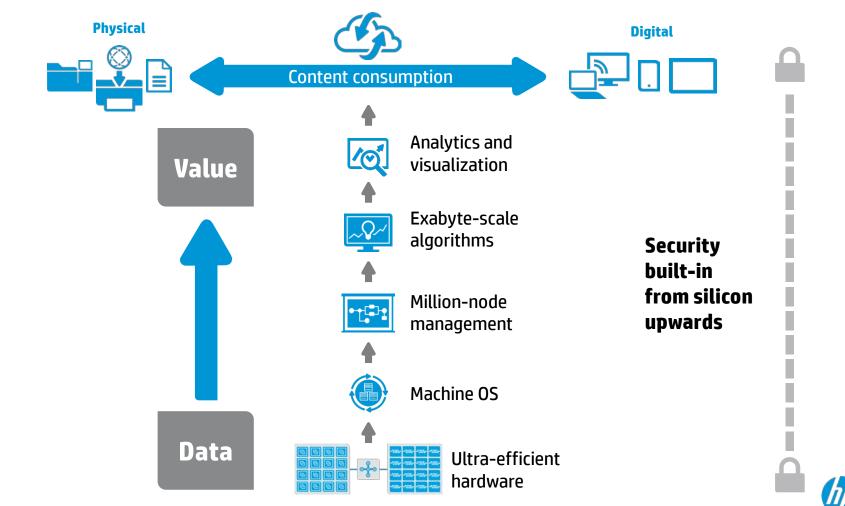




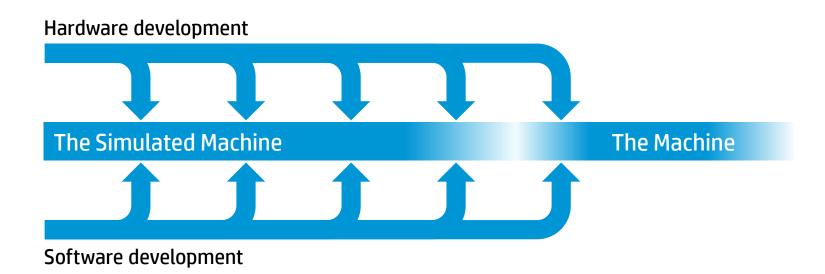
system with its own hierarchy







Hardware/software co-development





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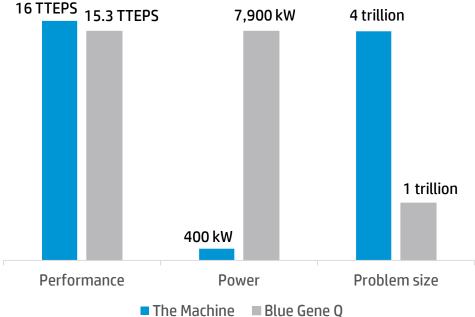
Software	
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MISC - misc commands	
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address: 0x0000000001c00000	
IvyBridge 2 (cell 0, socket 0, core 1, thread 0): Status = Low Power M	ONITOR
address: 0x00000001ba31e000	
IvyBridge 32 (cell 0, socket 1, core 8, thread 0): Status = Low Power M	ONITOR
address: 0x00000001ba328000	
IvyBridge 34 (cell 0, socket 1, core 1, thread 0): Status = Low Power M	ONITOR
address: 0x0000001ba32a000	
IvyBridge 1024 (cell 4, socket 8, core 8, thread 8): Status = Low Power M	ONITOR
address: 0x0000000001c00000	
IvyBridge 1026 (cell 4, socket 8, core 1, thread 0): Status = Runnable	
IvyBridge 1056 (cell 4, socket 1, core 8, thread 0): Status = Low Power M	ONITOR
address: 0x06060601ba218060	
IvyBridge 1058 (cell 4, socket 1, core 1, thread 0): Status = Runnable	
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	00000004007f8	SimApi	SEQ2				
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Performance estimates – graph traversal

What could you do if you could traverse 16 trillion graph edges per second?



Graph 500-like workload

Sequoia, Blue Gene Q at Livermore

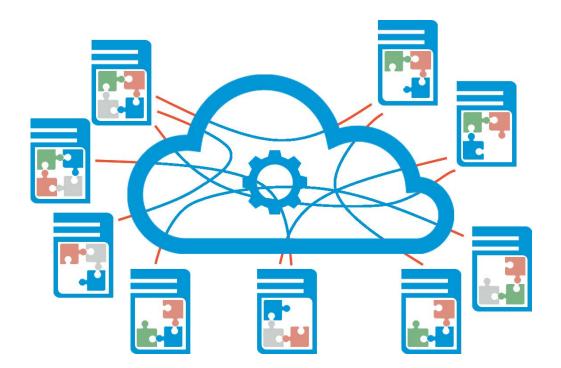
64,000 nodes, > 1M cores total

HP – The Machine

20 racks, 256 SoCs / rack, 122k cores total

256 GB NVM per SoC, 1.3 PB total 256 NICs per rack, 2*100 Gbps links / NIC Utilization < 70%

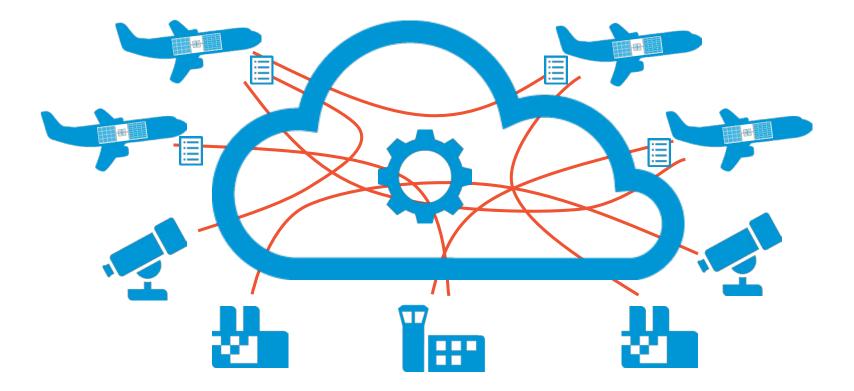




Translator Coordinator Orchestrator Arbitrator Aggregator Replicator Anonymizer **Border guard** Learning engine

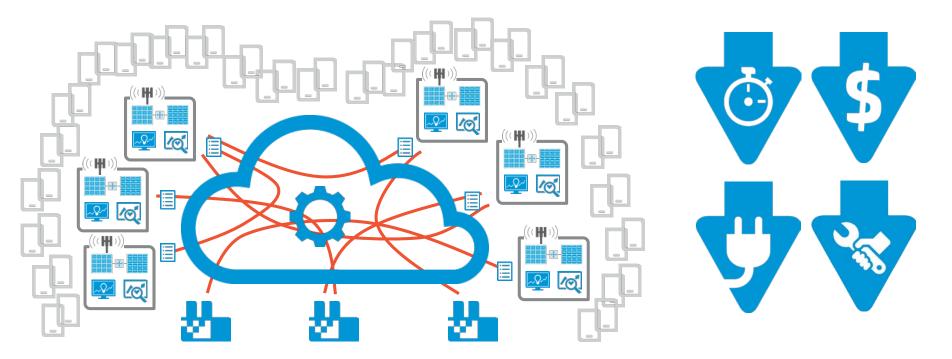


A mesh of connected aircraft ...





Use case: the smart cell tower





Future History

·UUI-	•UUL+ •UUL+				
•MU+ •MU+	•UUL+ •UUL+				
•UUL+ •UUL+	•UUL+ •UUL+				
•UUL+ •UUL+	•UUL+ •UUL+				

- Memristors begin sampling
- Physical infrastructure of Core prototypes established
- Open Source Machine OS SDK and emulators released
- ISV Partner collaborations begin

2015

- Edge devices begin sampling
- Machine OS enters public beta

2017

- Core devices at volume
- Machine available as product, service, and as a business process transformation

2019

 Memristor media controller, protocols and standards established

> SoC Partners selected for co-development

2014

 Machine OS development begins Memristor DIMMs launched

2016

 Integrated core technologies demonstrated • Edge devices ship in volume

2018

- Core Machines running real-world workloads at scale
- Machine OS released

• Distributed mesh cloud goes mainstream

2020



This changes everything





The Machine

Resources to share with customers

The Machine External Webpage

The Machine (German) 3 min video

The Machine classic 3 min video

Memristor Lab Tour

Photonics Lab Tour

HP Analytics Lab

HP Security and Cloud Lab

